

## Steep-Slope Devices with Mechanism Engineering for Steep Switching and Improved Driving Capability

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With CMOS technology continues scaling, the standby power becomes higher than the active power. Much attention has been paid to new devices with ultra-steep subthreshold slope (SS less than 60mV/dec at room temperature), which can effectively reduce the leakage current. The tunneling FET (TFET), which features as a gated p-i-n structure and is switched by band-to-band tunneling (BTBT), shows great potentials for steep SS, low off-current  $I_{OFF}$  and reasonably low operating voltage. However, it is difficult to form abrupt doping profile in the experiments for sharp band bending and thus relatively large SS of experimental demonstrations compared with the ideally theoretical expectations. Another critical issue is the on-current  $I_{ON}$  is relatively low for silicon-based TFET due to the poor tunneling efficiency. People have made a lot of efforts to solve these issues in terms of material, structure and process, including adoption of small-bandgap materials, hetero-junction, multi-gate structure with thin body, inserting pocket and advanced junction technology, etc..

Mechanism engineering is focused in this paper as a different possible way to solve the issues. Two kinds of newly-proposed all-silicon TFETs which have compatible process are discussed. One is the Si junction-modulated TFET (JTFET) with the equivalent function to achieve more abrupt doping profile by a kind of self depletion effect, rather than advanced junction technology, which results in steeper SS with experimental demonstration. An additional self-depleted pocket is introduced to further reduce SS of JTFET. Compared with other pocket TFETs, the pocket design in the proposed JTFET can be much relaxed with only regular implantation and annealing process needed for the pocket formation. The fabricated Si poc-JTFET exhibits very small  $SS_{min}$  of 36mV/dec, with good saturation behavior for output characteristics.

Another device we proposed is multi-finger-gate TFET of dopant-segregated Schottky Barrier source (mFSB-TFET). The device has the dopant-segregated Schottky (DSS) source, a comb-shaped gate with multiple fingers connected with the DSS source to form the Schottky junction. The device can realize a kind of adaptive operation mechanism for better performance tradeoff: with higher ON-current by the dominant Schottky current, appreciably reduced off-leakage current by self-depletion effect, steeper SS by dominant band-to-band tunneling over SB current and enhanced source surface electric field from the coupling effect between multi-fingers. With further improvement on SOI substrate, the fabricated silicon-based device with the same footprint can achieve  $I_{ON}$  by about two magnitude orders higher than traditional TFET, steeper SS over 5.5 decades of current and a minimum SS of below 60mV/dec, as well as higher  $I_{ON}/I_{OFF}$  ratio of  $10^8$ .

Due to the inherent advantages from principle engineering, the proposed devices can be further extended and combined with other material/structure/process improve methods for even better tradeoff of the properties of TFETs.

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