Invited Paper

Novel Wide Bandgap Semiconductor Ga_2O_3 Transistors

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We present the current status of transistor technology development based on new oxide compound semiconductor, gallium oxide (Ga_2O_3). We have been proposing Ga_2O_3 as a promising candidate for power device applications because of its excellent material properties and suitability for mass production [1]. The 4.8-eV bandgap and the Baliga's figure of merit of Ga_2O_3 are much larger than those of SiC and GaN, which will enable Ga_2O_3 power devices with higher breakdown voltage (V_{br}) and efficiency than SiC and GaN devices. The other important advantage of Ga_2O_3 is that a single-crystal bulk can be grown by using the same melt growth methods as are used for sapphire. Therefore, Ga_2O_3 power devices have the obvious potential to surpass SiC and GaN in not only device performance but also cost effectiveness. First, we succeeded in demonstrating metal-semiconductor field-effect transistors (MESFETs) using a single-crystal Ga_2O_3 channel grown on a β-Ga_2O_3 (010) substrate [1]. The MESFET showed excellent device characteristics such as a three-terminal off-state V_{br} of 250 V and a drain current (I_d) on/off ratio of about four orders of magnitude. However, the device suffered from high contact resistance of source and drain electrodes. In addition, its I_d on/off ratio was limited by a small leakage current through the unpassivated Ga_2O_3 surface. Recently, we fabricated Ga_2O_3 metal-oxide-semiconductor FETs (MOSFETs) with an *n*-type Sn-doped channel layer grown by molecular-beam epitaxy (MBE) that overcame the drawbacks of the MESFETs [2].

Depletion-mode Ga_2O_3 MOSFETs were fabricated on Fe-doped semi-insulating single-crystal β-Ga_2O_3 (010) substrates. A Sn-doped *n*-Ga_2O_3 channel layer with a thickness of 300 nm was grown on the substrate by MBE. Figures 1(a) and (b) show a cross-sectional schematic illustration and an optical micrograph of the Ga_2O_3 MOSFET, respectively. Multiple Si-ion implantations were performed to the regions for source and drain electrodes to form a 150-nm-deep box profile with Si=5×10^{19} cm^{-3}, followed by activation annealing at 925°C for 30 min. Then, a Ti/Au metal stack was deposited on the implanted regions and annealed at 470°C for 1 min. The specific contact resistance as measured by the circular transmission-line method was as low as 8.1×10^{-6} $\Omega\cdot cm^2$. A 20-nm-thick Al_2O_3 gate dielectric and passivation film was formed on the Ga_2O_3 layer at 250°C by plasma atomic layer deposition. The gate metal was formed with Ti/Pt/Au on top of the Al_2O_3 film. The gate width, source-drain implant spacing, and diameter of the inner circular drain electrode were 500, 20, and 200 µm, respectively.

Figure 2(a) shows the DC output characteristics of the Ga_2O_3 MOSFET measured at room temperature. The I_d was effectively modulated by the gate voltage (V_g) with good saturation and sharp pinch-off characteristics. The maximum I_d was 39 mA/mm at V_g=+4 V. The three-terminal off-state V_{br} was as high as 370 V at V_g=-20 V. The transfer characteristic of the MOSFET at a drain voltage (V_d) of 25 V is shown in Fig. 2(b). The I_d on/off ratio was extremely high, exceeding ten orders of magnitude with the measured off-state leakage reaching the lower limit of the measurement instrument. These Ga_2O_3 MOSFET characteristics were much better than those of the Ga_2O_3 MESFETs we had reported previously [1]. Figure 3(a) illustrates the temperature-dependent transfer characteristics of the MOSFET at V_d=25 V. The corresponding I_d on/off ratios, defined as the I_d at V_g=0 V divided by the I_d at V_g=-25 V, are plotted in Fig. 3(b). These device characteristics evolved smoothly with increasing device operating temperature. No kinks or abrupt changes that might be indicative of breakdown events and/or permanent degradation were observed, suggesting stable device operation in the whole temperature range from 25 to 250°C. The MOSFET maintained a high I_d on/off ratio of approximately four orders of magnitude even at 250°C as shown in Fig. 3(b). All these device characteristics indicate that the Ga_2O_3 MOSFET can perform at elevated temperatures up to at least 250°C without noticeable irreversible degradation.

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References

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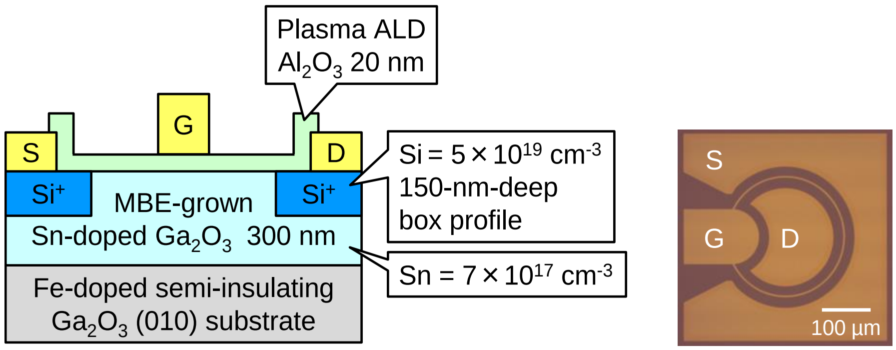
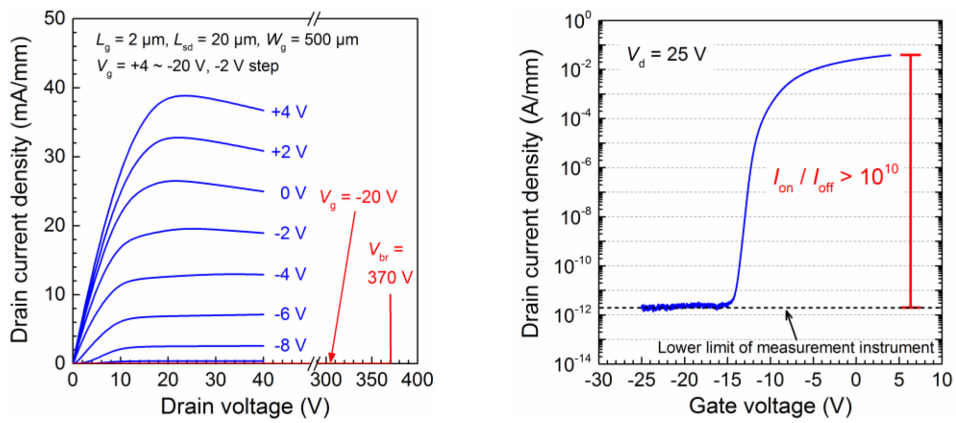


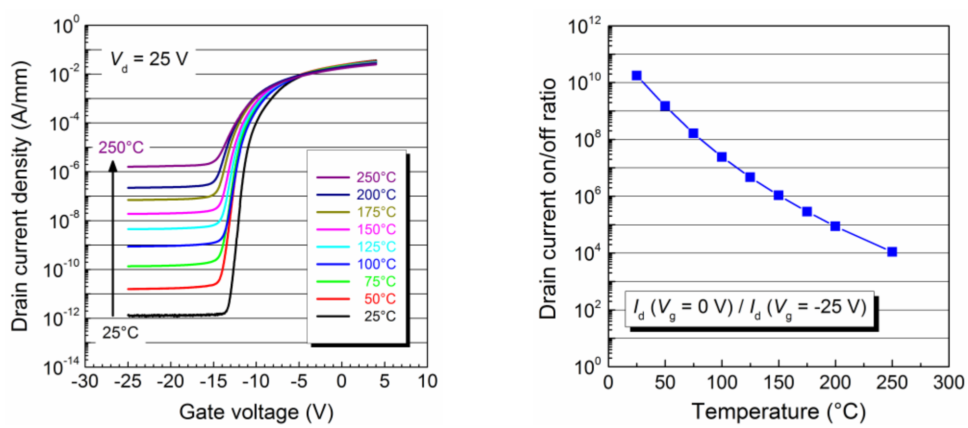
(a) (b)

Fig. 1: (a) Schematic cross section and (b) optical micrograph of depletion-mode Ga_2O_3 MOSFET.



(a) (b)

Fig. 2: (a) DC output and (b) transfer characteristics of Ga_2O_3 MOSFET.



(a) (b)

Fig. 3: (a) Transfer characteristics and (b) I_d on/off ratios of Ga_2O_3 MOSFET as a function of temperature.