Student Paper

Carrier Transport Phenomena in Cylindrical Channel III-V Gate-All-Around Nanowire Transistor

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Gate-all-around (GAA) structure has already been proven as one of best options to restrain short channel effects (SCEs) [1-2]. In addition when it is combined with III-V channel material and high-k gate dielectric, GAA device holds the potential to be used in future ultra-high performance devices with all-around on and off state performance. On that note, III-V high-k GAA with rectangular cross section has been demonstrated experimentally by Gu et al. [3], which shows excellent transport performances as expected. Recently we have reported the electrostatics of that rectangular GAA device through rigorous self-consistent Schrodinger-Poisson simulation [4]. In this paper, we extend our work by solving the electrostatics of a cylindrical channel III-V GAA FET along with transport study in ballistic regime.

The device under study (Fig. 1a) has a cylindrical $In_xGa_{1-x}As$ p-doped channel surrounded by a 10nm thick Al_2O_3 oxide layer. The cross sectional area of the channel was kept equal to the area of the rectangular GAA device channel examined earlier [4].

A 2-D self-consistent numerical model based on finite element method is developed, which solves Schrodinger-Poisson in a coupled manner for a vertical cross section of the device at the source end (Fig. 1b), in polar co-ordinate system. Upon convergence the model provides Eigen energies, carrier density, capacitance-voltage and other electrostatic characteristics. Figure 2 demonstrates the C-V characteristics along with ATLAS verification, which confirms the validity of the simulator developed. It is to be mentioned that, the C-V characteristics from the cylindrical (this work) and rectangular channel [4] cross section GAA is found to be almost identical, as expected [5].

The electron concentration profile (Fig. 3) at strong inversion region reveals that for cylindrical channel, the inversion layer forms uniformly just beneath the oxide interface, unlike the rectangular channel GAA device where the peaks of electron concentration is at the corners [4]. Large electron concentration at corner means large voltage drop and band bending at the corners, which implies that rectangular channel FET will have more gate leakage than the cylindrical counterpart through the corners.

The obtained Eigen energies from the self-consistent model are used to calculate the drain current using the well-known Landauer-Buttiker formula-

$$I = \frac{2e}{h} \int_{-\infty}^{+\infty} T(E)\,(f_1(E) - f_2(E))\,dE \tag{1}$$

Here, the transmission coefficient T(E) is assumed to be step-like, meaning the resultant current is for ballistic regime. Figure 4 and 5 respectively shows the output and transfer characteristics of this cylindrical channel GAA device. Because of the 2–D simulation, which does not take account of the drain voltage effect, the effect of DIBL is not visible in the I_d-V_{ds} curve of the device. Finally, Table 1 summarizes few performance parameters extracted from the transport study. The device shows excellent sub-threshold slope (SS) and on/off current ratio. On the other hand, peak saturation current and trans-conductance are also quite satisfactory.

In summary, this work reports a self-consistent physical model to investigate the electrostatics and transport properties of a cylindrical channel GAAFET, revealing the fact that although the carrier concentration profile is completely different for cylindrical and rectangular channel GAAFET, there is only subtle variation in capacitance and magnitude of drain current. In addition, various performance parameters are extracted which indicates promising on and off state performance of the cylindrical channel GAAFET.

References

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[4] Q. D. M. Khosru et al., "Capacitance-Voltage Characteristics of Gate-All-Around $In_xGa_{1-X}As$ Nanowire Transistor," *ECS Transactions*, vol. 53, no. 1, pp. 169-176, May 2013.

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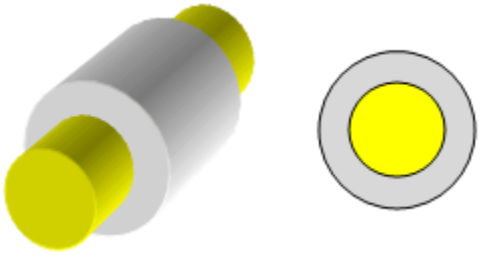

(a) (b)

Figure 1. (a) Device under study with outer oxide thickness of 10nm and channel radius of 16.93nm (b) cross section considered for simulation taken at source end to avoid drain voltage effect.

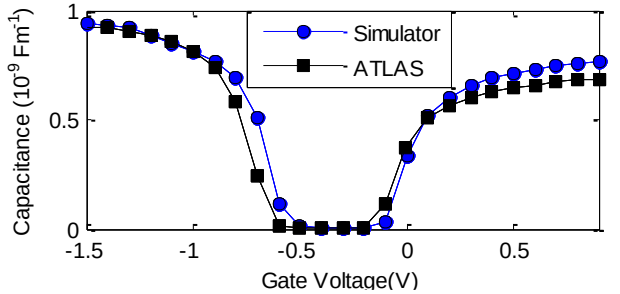

Figure 2. Capacitance-voltage characteristics of the device along with ATLAS verification. The capacitance is for per unit channel length since only 2-D cross section is considered.

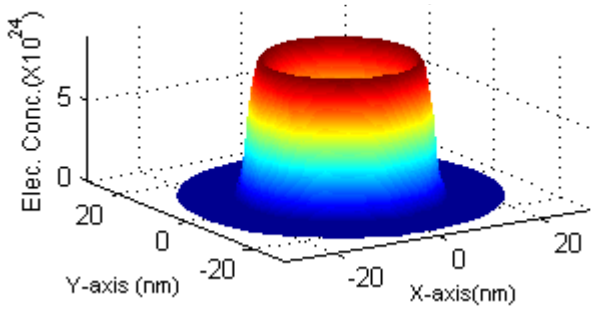

Figure 3. Electron concentration (m^{-3}) in the device at Vgs=1V, revealing an all-around channel formation just beneath the oxide-semiconductor interface.

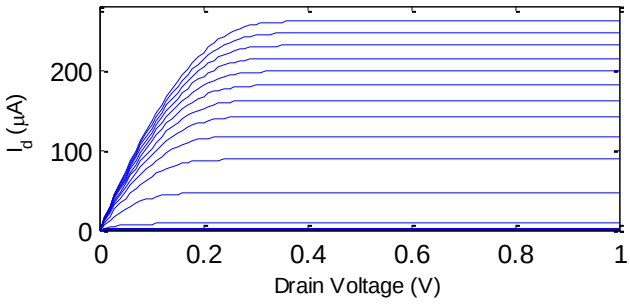

Figure 4. I_d-V_{ds} curve for the device with gate voltage range from -1.5V to 1V with 0.1V interval.

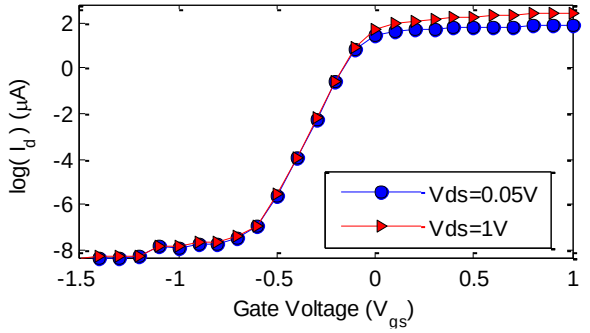

Figure 5. Transfer characteristics of the device under different drain bias.

TABLE 1. Transport Performance Parameters

Threshold Voltage (V)	**SS** (mV/dec)	**I_{on}/I_{off}**	**Peak Sat. Curr.** (μA)	**Max g_m** (A/V)	**On resist.** (Ω)
-0.25V	63 @ Vds=0.05 V	4.3 x 10^4	260.6 @ Vgs=1 V	0.42 x 10^{-3} @ Vds=1 V	703 @ Vgs=1 V