Invited Paper

Energy in (Nano)Electronics: Examples from Graphene to Phase-Change Memory Devices

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Energy use and conversion are important for the design of low-power electronics and energy-conversion systems. This is also a rich domain for both fundamental discoveries as well as technological advances. In the realm of electronics, energy and power consumption limit applications ranging from mobile devices (~10^{-3} W) which are battery-limited, to large data centers (~10^{6} W) which must be co-located with power generation facilities [1]. Interestingly, total data center energy consumption in the US alone is estimated at approximately 10 GW, and in the world it is approximately three times larger.

This talk will present recent highlights from our studies of energy dissipation and transport in novel nanoelectronics. We have investigated both Joule heating [2,3] and Peltier cooling [4] in graphene transistors and suspended graphene [5], thermal transport in graphene nanoribbons (GNRs) [6], and engineering of high-field current transport in graphene interconnects [7]. For instance, Fig. 1 shows that graphene transistors (GFETs) heat up non-uniformly during high-field operation, due to varying carrier density and electric field along the channel. A hot spot forms at the location of maximum field (minimum carrier density), and its position depends on the applied voltages [2].

We have also uncovered that thermal transport in "short" (i.e. sub-micron length) GNRs can approach ballistic heat flow limits at room temperature, while the thermal conductivity of "narrow" (sub-200 nm width) GNRs is strongly diffusive and limited by edge scattering, approximately as ~W^2 (where W is the GNR width) [6]. These findings have important implications for the use of graphene nanoscale devices and interconnects of dimensions comparable to the electron and phonon mean free paths (~20 nm and ~100 nm for SiO_2-supported graphene at room temperature, respectively) [6].

In addition to the above, we have examined fundamental limits of data storage based on phase change (rather than charge or spin), achieving energy dissipation two orders of magnitude below industry state-of-the-art, approaching femtojoules per bit [8,9]. We have achieved this by using individual carbon nanotube (CNT) electrodes to contact phase-change memory (PCM) bits of dimensions near 10 nm, the smallest achieved to date. By nanoscale thermometry we have also found that Peltier effects play an important role in the operation of such nanoscale PCM cells [10].

The results suggest new directions to improve nanoscale energy efficiency in electronics towards fundamental limits, through the co-design of geometry and materials.

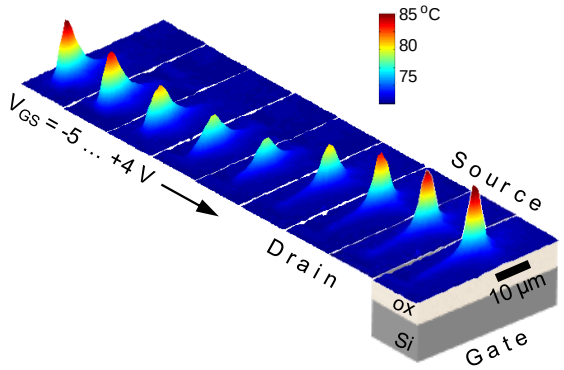

Fig. 1. Infrared (IR) thermal imaging of graphene field-effect transistor (GFET) during operation, from [2]. The figure is a sequence of IR images taken at varying gate voltages (V_{GS}) as labeled, and V_{DS} = 12 V. A hot spot forms at the location of highest field, and "moves" along the channel as the voltages are varied, and the transport changes from unipolar (n- or p-type) to ambipolar [2].

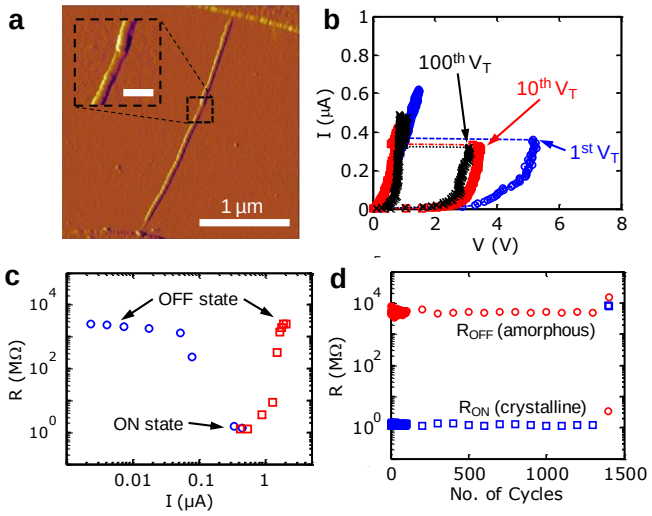

Fig. 2. Phase-change memory (PCM) devices with carbon nanotube (CNT) electrodes [8,9]. (a) AFM image of device. Inset zoom-in shows bit region (scale bar 150 nm). (b) Electrical characteristics of the 1st, 10th and 100th SET switch, showing the threshold voltage stabilizes at V_T ~ 3.2 V. (c) Resistance switching after a series of current pulses with increasing amplitude. The switching power is the lowest achieved to date on PCM. The ratio R_{OFF}/R_{ON} = 2.5 GΩ/1.3 MΩ, nearly ~2000×. (d) Endurance test for ~ 1500 cycles.

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