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Invited Paper

Conductive Atomic Force Microscope as a Tool for the Characterization of Time-Dependent Variability of MOS Devices: Two Case Studies

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Conductive Atomic Force Microscopy (CAFM) has been demonstrated to be a very effective technique in providing detailed information on the morphological and electrical properties and failure mechanisms [1,2] of the gate dielectric of MOS devices from its characterization at the *nanoscale*. However, because of experimental difficulties, few efforts have been done to establish a correlation between the observed *material properties* and the *electrical performance and reliability of electron devices*. In this work, two case studies will be described to demonstrate that a well designed experiment, which combines standard electrical tests and CAFM measurements on the suitable test structures, can help in setting the nanoscale origin (technological and/or physical) of the observed device behavior.

The impact of the *poly-crystalline* structure of a high-k material on the variability, performance, aging and TDDB of MOS structures has been analyzed. *MOS capacitors* with an Al gate electrode and a nominal 3.6nm thick HfO_2 film (grown by ALD) as gate dielectric were first considered. Before Al deposition, some of the samples were annealed at 350° or 800°C. Larger pre-BD currents and sample-to-sample variability and reduced reliability were observed on the 800°C annealed structures (Figure 1) [3]. Topography and current images were measured with the CAFM after removing the Al gate, on as-grown and CCS stressed devices. The sample annealed at 800°C shows a granular structure (Fig.2.right), which has been attributed to the presence of randomly oriented nanocrystals (NC) separated by grain boundaries (GBs) [3]. These samples also show larger inhomogeneities of the conductivity (larger rms current values), which considerably increases after stress (Table in Fig. 2) [4]. All these results suggest that the polycrystallization of the high-k layer is an important source of device time-dependent variability. To further analyse this point, optimized HfO_2 stacks were fabricated. The nanoscale results demonstrate a clear correlation between topography and current (Fig. 3) [5] and contact potential difference (CPD) [6], showing larger currents and CPD (indicative of positive charge trapping) at the GBs. Moreover, under electrical stress, the GBs degrade faster than the grains (Fig. 4) and are preferential BD locations [6]. Then, the higher initial currents at the GBs could be related to the higher concentration of positive charges there, likely associated with the segregation of positively charged oxygen vacancies. Larger voltages would be applied to the underlying SiO_2 interfacial layer at the GBs, leading to a faster degradation there, eventually leading to the BD of the entire stack [7].

The nanoscale differences in the aging of *MOSFETs* after Bias Temperature Instability (BTI) and Channel Hot Carrier (CHC) Injection stresses have been evaluated on pMOSFETs (WxL=0,5μm x1μm) with a 1.4nm thick SiON layer as gate dielectric. After the BTI or CHC stress (Fig. 5), the layers on top of the gate dielectric were removed with a very selective wet etch, to expose the gate dielectric (Fig. 6). The CAFM current images (Fig. 7) suggest that (i) the number of leaky sites on the stressed MOSFETs is considerably larger and (ii) the distribution of leaky sites over the gate region depends on the kind of previous stress, being preferentially located close to the drain and source on the CHC pre-stressed MOSFETs (Fig. 8). TCAD simulations show that, under CHC stress, aging is caused by the combination of electric field and impact ionization effects (Fig. 8) [8], suggesting permanent damage caused by NBTI in the region close to source and hot-carrier injection close to the drain.

References

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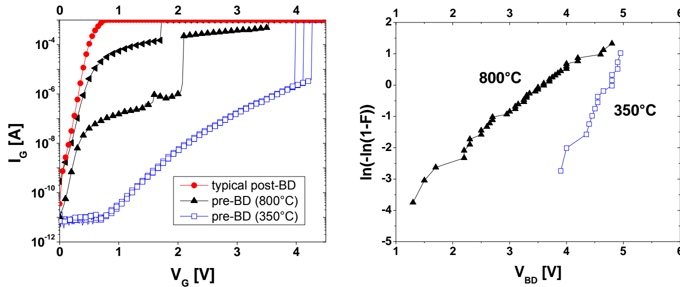
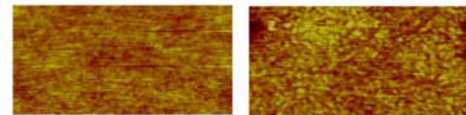


Fig 1. Left. Examples of I-V curves measured on several MOS capacitors (9µm² area, Al electrode) with a 3.6 nm thick HfO_2 layer, after annealings at 350° or 800°C. Right. Weibull plot of the breakdown voltage measured from ramped voltage stresses. [3].



	350°C	800°C
Before stress	0.27pA	0.36pA
After stress	0.36pA	4.45pA

Fig. 2. Topography images of HfO_2 layers (Fig. 1) annealed at 350° (left) and 800° (right). Size is 1x0.5µm^2. Table. rms values of the current (measured from the CAFM current images) before and after a CCS stress [4].

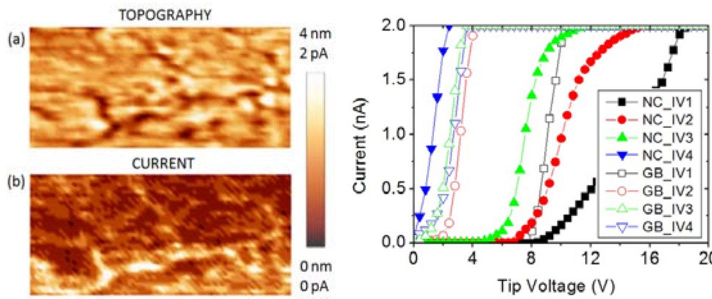


Fig. 3. Topography (a) and current (b) measured on optimized HfO_2 stacks [5]. Images size is 140nm x 300nm.

Fig. 4. Evolution of the current through the grain (NC IV) and GB (GB IV) during sequential CAFM I-V measurements on the same spot [6].

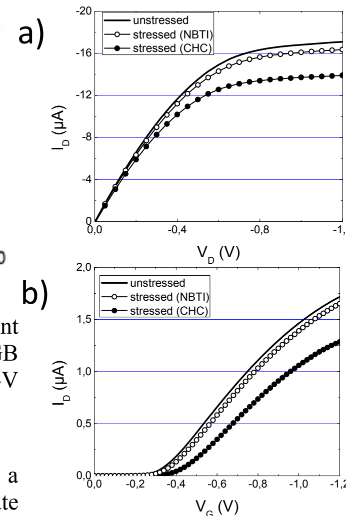


Fig. 5. Typical I_D-V_D (a) and I_D-V_G (b) characteristics of MOSFETs measured before (line) and after CHC (solid symbols) or BTI (open symbols) stress [8].

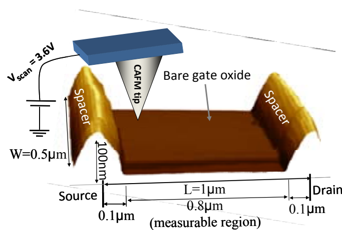


Fig. 6. Topography image of a pMOSFET after removal of the gate electrode, showing a very flat surface between the two spacers. The dimensions of the studied area and the structure polarization are indicated [8].

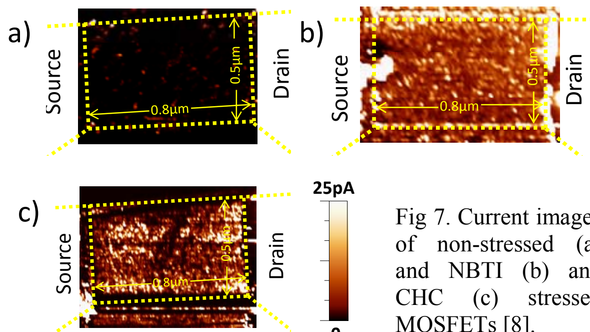


Fig 7. Current images of non-stressed (a) and NBTI (b) and CHC (c) stressed MOSFETs [8].

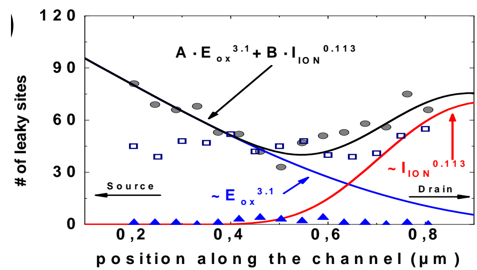


Fig. 8. Average number of leaky sites obtained at different positions along the channel in a fresh (triangles), NBTI (squares) and CHC (circles) stressed device, obtained from the current images in Fig. 7. Lines correspond to the fitting of the number of leaky sites to $A \cdot E_{ox}^{\gamma}$ (blue) and $B \cdot I_{ion}^{\alpha}$ (red) and their sum (black) [8].