Student Paper

ZnO Thin Film Transistors for Extreme Environment Applications

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Oxide-based semiconductors have rapidly developed in recent years for thin-film transistor applications. These materials are of interest because their low deposition temperature, high mobility, and good electrical stability make them an attractive alternative to amorphous silicon for large-area thin film electronic applications. In this work, we use a simple low-temperature deposition technique, plasma-enhanced atomic layer deposition (PEALD), to deposit high quality ZnO films for thin film transistors.We report and compare the effects of ^{60}Co gamma ray irradiation on ZnO TFTs with and without electrical bias. We also note measurement artifacts due to air ionization and routes to minimize such effects.

We previously reported gamma ray radiation exposure results for electrically unbiased ZnO TFTs and circuits and found only small electrical changes for doses up to 100 Mrad [1]. We have also reported on the effects of electrical bias and irradiation on ZnO TFTs for doses up to 25 Mrad [2]. Irradiation induced changes for both biased and unbiased TFTs are nearly completely removed by a 60 s anneal at 200 °C and decay even at room temperature. The ZnO TFTs used in this work have a bottom gate structure (Figure 1, left) and were fabricated on borosilicate glass substrates. 32 nm thick Al_2O_3 as gate dielectric and 10 nm thick ZnO as active layer were deposited at 200 ºC by PEALD on patterned Cr gates. Titanium source and drain contacts were deposited by sputtering and patterned by lift-off, and a 32 nm ALD Al_2O_3 passivation layer was deposited to complete the devices. A simple 4 x 4 TFT array (Figure 1, right), was used to allow biasing of multiple devices. Figure 2 (left) shows I_{DS} versus V_{GS} pre- and post-irradiation transfer characteristics of TFTs with 25 Mrad cumulative dose. A comparison is made between devices biased at V_{DS} = 6.0 V and V_{DS} = 0.5 V with V_{GS} = -6 V except during device V_{GS} sweeps (one sweep every 140 seconds, 0.5 Mrad/hour fluence). The change in V_{ON} is identical for both bias conditions. The saturation current is nearly unchanged before and after irradiation. The turn-on voltage shifts negative by ~1 V for both V_{DS} = 6.0 V and V_{DS} = 0.5 V. Figure 2 (right) shows the extracted threshold voltage as a function of irradiation dose for both irradiation only and for electrical bias while irradiation. The threshold voltage shifts negative for moderate dose and the shift saturates at higher dose (>20 Mrad).

For devices under irradiation with electrical bias, the subthreshold current increases during irradiation, but immediately returns to its pre-irradiation value when removed from the gamma ray flux, suggesting a measurement artifact during irradiation. It is also apparent that most of the changes occurring in the ZnO devices occur for small dose. To better understand these effects, we measured devices with lower exposure fluence (0.1 Mrad/hour). The TFTs used in this work have a bottom gate device structure. This structure leaves the back channel surface exposed to the environment or protected with a passivation layer, as shown in figure 1 (left). In this work, the irradiated devices are measured in air. Because of the gamma ray flux the air surrounding the TFTs is partially ionized, when the TFT is in its OFF stage (< -1V), the negative gate voltage will attract positive ionized charge at the back surface. This charge will shift the device characteristics negative and will be seen as an apparent increase in subthreshold current. The charge is only partially bound and even a positive gate voltage is sufficient to remove much of the charge. To confirm this origin for the transient subthreshold characteristic we grounded the back interface of the TFTs and exposed them to low doses of ^{60}Co (Figure 3, left). Devices were measured during irradiation (Figure 3, right). The first sweep with irradiation shows a small increase in subthreshold current, but this current is greatly reduced for subsequent V_{GS} sweeps throughout the gamma ray exposure. The devices show virtually no shift in V_{TH} during or after exposure for a cumulative dose of 240 Krad. This suggests ZnO TFTs are excellent candidates for use in extreme radiation environments.

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References

[1] Zhao D.A. et al., Gamma-ray Irradiation of ZnO Thin Film Transistors and Circuits. *Device Research Conference*, p. 241-242 (2010)

[2] Ramirez J. I. et al. Effects of Gamma-Ray Irradiation and Electrical Stress on ZnO Thin Film Transistors. *Device Research Conference*, (2013)

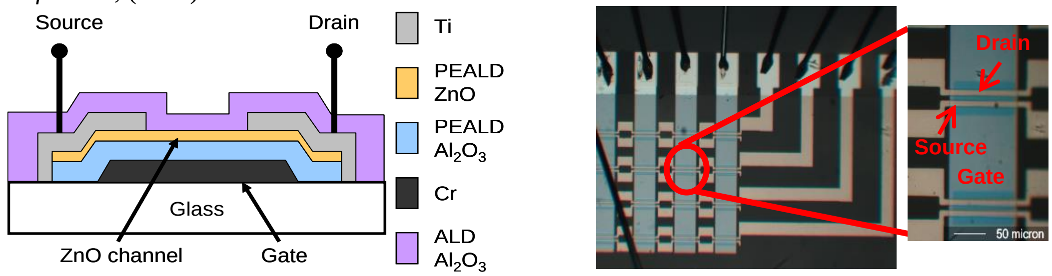

Fig. 1: (left) Bottom gate ZnO TFT schematic cross section; (right) optical micrograph of 4 x 4 ZnO TFT array used in electrical bias and radiation measurements

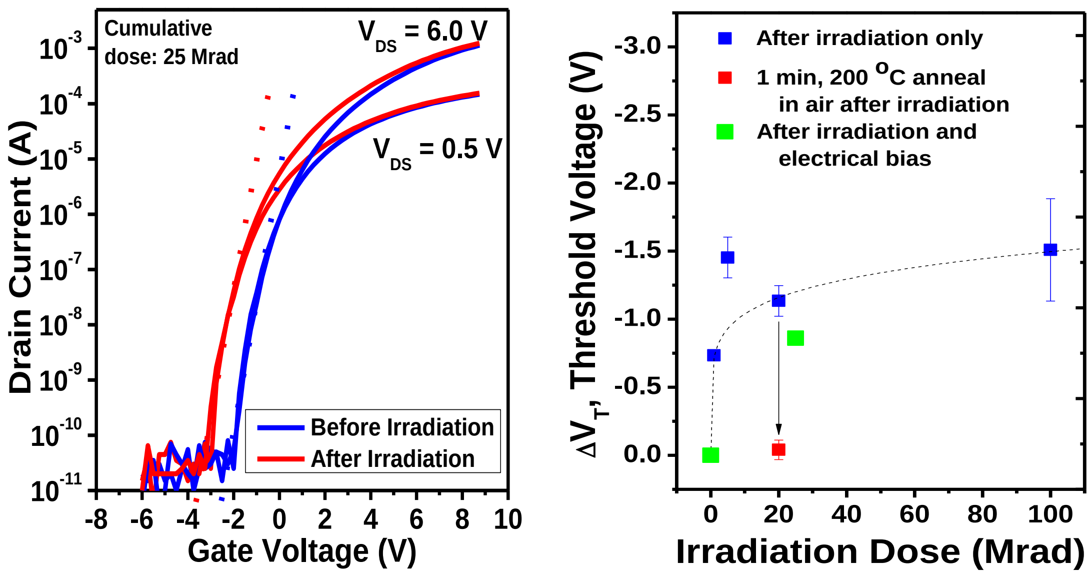

Fig. 2: (left) Linear region(V_{ds} = 0.5 V) and saturation region (Vds = 6V) log(I_D) versus V_{GS} of ZnO TFTs pre- and post- irradiation for a cumulative ^{60}Co dose of 25 Mrad. Device dimensions are W/L = 100 μm/5μm. (right) Threshold voltage as a function of irradiation dose for irradiation only and irradiation with electrical bias. In both cases, threshold voltage shift is similar.

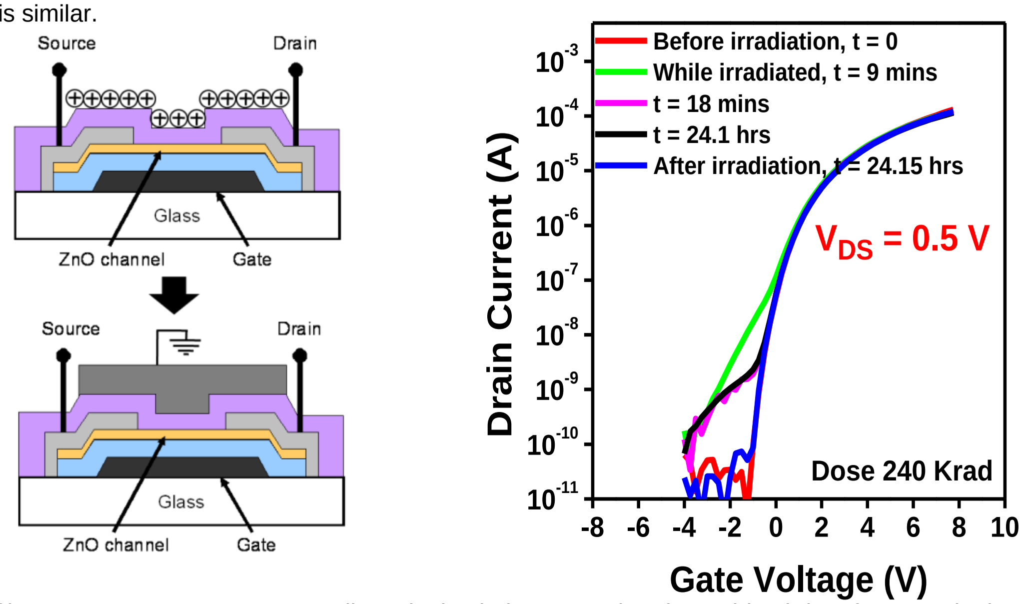

Figure 3: (left) Bottom-gate TFT structure collects ionized charge on the channel back interface. Back channel was grounded to avoid ionized charge to be collected. (right) Linear region (V_{ds} = 0.5 V) log(I_D) versus V_{GS} for a cumulative ^{60}CO dose of 240 Krad with the back channel surface grounded to avoid collection of charge at the surface.