Voltage Doubler Design Procedure for Low Ambient RF Energy Harvesting Applications

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I. Introduction

Digital electronics continues decreasing its power consumption without sacrificing performance because process technology shrinks transistor sizes as Moore law predicted in the last few decades. Analog electronics also keeps decreasing its power consumption by taking advantage of the device scaling, as well as newly developed power efficient circuit techniques. For example, the recently reported low power radio frequency (RF) receiver with an integrated low drop-out voltage regulator only requires 4mW power consumption with -60dBm sensitivity operating at a 1Mbits data rate with a 2.4 GHz carrier frequency [1]. Furthermore, a low power FSK receiver was recently reported [2] which consumes as little as fraction of a mW of power. As transceiver power consumption keeps approaching the level of the ambient energy source such as radio frequency (RF) energy [3], energy harvesting emerges as a promising power solution for low power electronics. These low power electronic circuits need to operate for a few month or years without maintenance to enable different environmental sensor applications, and could be integrated into the internet of things (IoTs) to form a smart house in the future by being able to harvest their power needs directly from the environment. This has a huge market potential and has attracted research [1-4].

Recent RF energy harvesting work has demonstrated 9 percent efficiency using voltage boosting and self-biasing network techniques [3-4] at two different bands at ambient power levels. A high efficiency dual band pitch antenna has been developed which can be easily fabricated on a PCB board [5]. However, these previous works lack a detailed design procedure on how to size the basic energy harvester block: the voltage doubler which largely determines the harvesting efficiency.

This paper presents a detailed procedure on how to size the voltage doubler transistors to optimize AC to DC power conversion efficiency. It shows that there exists an optimal device size for a voltage doubler due to the tradeoff between voltage boosting and parasitic capacitance of the MOSFET connected diodes. Detailed design procedures have been provided.

II. Voltage Doubler Circuit Design Tradeoff

In low power RF energy harvesting applications, voltage boosting has been widely used to improve the conversion efficiency [3, 4] because of the low ambient power level. Figure 1 shows a one stage voltage doubler circuit for harvesting ambient RF energy. The voltage doubler uses the currents I_1 and I_2 to charge the capacitors C1 and C2. In ideal conditions, the output voltage V_{out} can be twice that of the V_{boost} voltage. Due to low environmental power, which is around or below -20 dBm in urban area [3], the input voltage is 30mV or even lower with a 50 Ohms load. Voltage boosting is an essential technique to achieve high conversion efficiency at low input ambient power level. The voltage boosting transforms the voltage to a level sufficiently high to turn on the rectifying active elements in the doubler circuit. The current I_1 and I_2 need to be increased to improve the conversion efficiency. The diode works in sub-threshold voltage region at the ambient power level. The current of a diode-connected MOSFET operating in the subthreshold voltage region can be described by Equation 1, where V_{ds} is the boosting input voltage, L is the inductor value and C_{para} is the parasitic capacitance of the inductor and the MOSFET connected diode (obtained from C_{gs}, C_{gb}, C_{db}), which is a function of the MOSFET size:

$$I_1(t) = \frac{W_{eff}}{L_{eff}} \mu C_d V_T^2 \exp\left(\frac{V_{ds}(t) - V_{th}}{nV_T}\right)\left[1 - \exp\left(-\frac{V_{ds}(t)}{V_T}\right)\right], 0 < V_{ds}(t) < V_{th}$$

$$V_{ds}(t) = V_{boost} = \sqrt{\frac{L}{C_{para}}} V_{in} \qquad (1)$$

In order to achieve high conversion efficiency, the charging currents (I_1 and I_2) need to be maximized. This is achieved by using a voltage boosting method which takes advantage of resonance and the intrinsic parasitic capacitance of the MOSFET to concentration power and turn on the device. According to equation 1, large device width increases the current, improves the conversion efficiency and may be preferred. On the other hand, a larger transistor width introduces larger parasitic capacitance which tends to reduce the boost voltage or V_{ds}. However, a large voltage across the diode connected MOSFET (V_{ds}) causes higher charging current I_1 and is thus preferred as well. The voltage boosting is determined by the ratio of the inductor (L) and parasitic capacitors (C_{para}). The parasitic capacitance of C_{para} comes from the parasitic capacitance of boosting inductor and parasitic capacitance of the MOSFET connected diodes. In order to obtain voltage boosting at desired frequency, equation 2 needs to be satisfied. This requires a constant multiplication product of capacitance and inductor at a fixed frequency. In order to improve the boosting ratio, a smaller parasitic capacitance and larger inductor size are preferred. There thus exists an optimal device width for a desired frequency in a specific process which optimizes charging current and charging voltage simultaneously

$$\omega = \sqrt{\frac{1}{L \times C_{para}}} \tag{2}$$

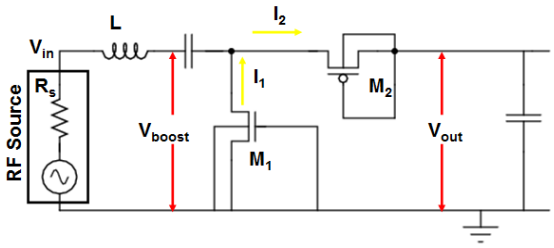

Figure 1. Voltage doubler using diode-connected MOSFETs.

III. Voltage Doubler Circuit Design Procedure

At a fixed ambient frequency, the first step is to choose the inductor size. For a given process, the high quality inductor needs to have a self-resonant frequency which is 20% to 30% higher than the harvesting frequency. The second step is to choose different width transistors in a range of 5 to 1000 times the minimal fabrication lengths. The width steps can be chosen in the following way: the next width is three to five times larger than the previous width. The resulting voltage doubler efficiency can be simulated and compared. An optimal width can be found to obtain maximum efficiency. A narrower device width range can then be chosen and the above procedure is repeated with smaller steps to find the optimal device widths. The inductor sizes can be chosen using a similar procedure to optimize the whole system conversion efficiency.

IV. Conclusions

RF energy harvesting represents a promising power source for future low power electronics which can enable wide sensor communication applications and can be integrated into the Internet of Things to form a smart house or structure. The voltage doubler is one of the key circuit blocks which determine the harvester conversion efficiency. Design equations have been provided to show the tradeoffs utilized in order to optimize the efficiency. Based on these equations, this paper demonstrates that there exists a set of optimal voltage doubler transistor sizes at a specific frequency. A detailed procedure is provided to find the optimal sizes of the MOSFET connected diodes to maximize the harvesting efficiency.

References

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