Analog/RF Performance of NPN SiGe HBT on Thin Film SOI Over -55 to +125 degC Temperature Range

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The research has been carried out to integrate MOSFETs and bipolar transistors on SOI substrate for high performance mixed signal applications [1]. Jin Cai, et al [2] analyzed npn SiGe HBT on SOI substrate. The characteristics of SiGe HBT on SOI over temperature range of 27 to 330 degC are reported in [3]. The performance of SiGe HBT on bulk is reported in extreme environment (-230 to 120 degC) in [4]. In this paper, the analog/RF characteristics i.e. AC voltage gain, power gain and unity current gain frequency of npn SOI HBT [5] is studied over temperature range of -55 to +125 degC in Sentaurus device simulator [6].

Fig.1 shows the schematic of a 0.15 X 1.0 μm^2 npn SiGe HBT on thin film SOI with parameters mentioned in Table 1. In this device structure, Ge profile was varied from 10 % (base- emitter junction) to 25 % (base-collector junction) to introduce an electric field in SiGe base. In the HBT simulation, the models that have been used are discussed in [5]. The Shockley-Read-Hall electron and hole lifetimes of SiGe are $3x10^{-6}$ s and $1x10^{-6}$ s respectively. The V_{CE} was kept 1.2 V and V_{BE} was varied from 0 V to 1.2 V during HBT simulation. The input DC characteristics and current gain were plotted over the temperature range of -55 to 125 degC as shown in Fig.3 and Fig.4 respectively. The small signal analysis of HBT has been performed with sinusoidal signal amplitude of 0.1(kT/q) at 1MHz frequency. From the analysis, the ac voltage gain (Y_{21}/Y_{22}) is evaluated (see Fig.5) over the specified temperature range. It has been observed that the performance to power consumption ratio of HBT is better at low temperature. The power gain, U of SiGe HBT on thin film SOI was obtained from the Y-parameters using formula from [7] (see Fig.6). The unity current gain frequency, f_t of the SOI HBT is shown in Fig.7. The f_t value of the HBT is better at low temperature due to high trans-conductance value.

The 2D numerical simulation of NPN SiGe HBT on thin film SOI within temperature range of -55^{0}C to 125^{0}C (military specification) has been performed. The DC current gain, AC voltage gain, power gain of HBT is analyzed with this temperature range. At low temperature, the improvement of voltage gain is attributed to high output impedance and high trans-conductance value of the HBT. To achieve same performance, HBT at low temperature consumes lower power compared to the HBT at high temperature. The simulation result suggests that npn SiGe HBT on thin film SOI can be used for analog/RF circuit applications within the specified temperature range which is of interest for military applications.

References

[1] T.H. Ning, “Why BiCMOS and SOI BiCMOS,” IBM Journal of Research and Development, Volume: 46, Issue: 2.3, pp.181-186, 2002.

[2] Jin Cai, et al, “Vertical SiGe-base Bipolar Transistors on CMOS-Compatible SOI Substrate,” IEEE BCTM, pp. 215-218, 2003.

[3] M. Bellini, John D. Cressler and Jin Cai, “Assessing the High-Temperature Capabilities of SiGe HBTs Fabricated on CMOS-compatible Thin-film SOI,” IEEE BCTM, pp.234-237, 2007.

[4] John D. Cressler, “Silicon-Germanium as an Enabling echnology for Extreme Environment Electronics,” IEEE transactions on device and materials reliability, vol. 10, no. 4, pp. 437-448, Dec. 2010.

[5] Prasanna Kumar Misra and S. Qureshi, “A Technique to Improve the Performance of an NPN HBT on thin filn SOI,” IEEE Journal of the Electron Devices Society, Vol. 1, No. 4, pp. 92-98, April 2013.

[6] Sentaurus device user guide, Version G-2012.06, June 2012.

[7] Behzad Razavi, Ran-Hong Yan, and Kwing F. Lee, “Impact of Distributed gate resistance on the performance of MOS devices”, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 41, Issue 11, pp.750-754, November 1994.

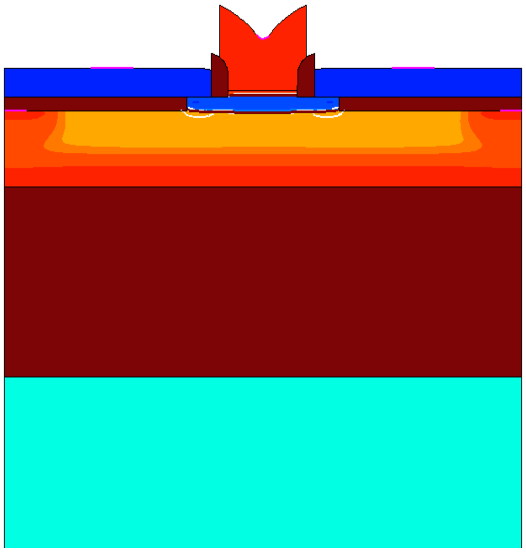

Fig. 1: Schematic of SOI HBT

Parameter	Values	units
Emitter thickness	100	nm
Emitter Width	150	nm
Base thickness	30	nm
Buried layer	40	nm
Deposited epi layer	120	nm
BOX thickness	400	nm
Emitter doping	1x 10^{20}	cm^{-3}
Base doping	1x 10^{19}	cm^{-3}
Epi layer doping	7.5x 10^{17}	cm^{-3}
Buried layer doping	5x 10^{19}	cm^{-3}
Substrate doping	1x 10^{15}	cm^{-3}

Table 1: SiGe HBT parameters

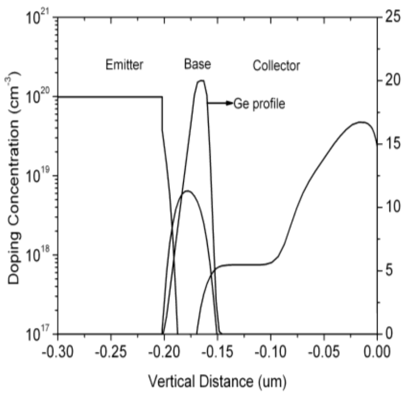

Fig. 2: Doping profile of SOI HBT

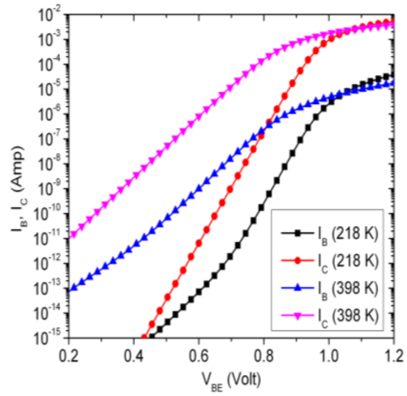

Fig. 3: Input DC characteristics of SOI HBT

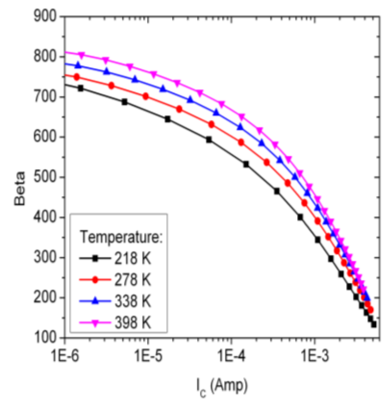

Fig. 4: Beta Value of SOI HBT

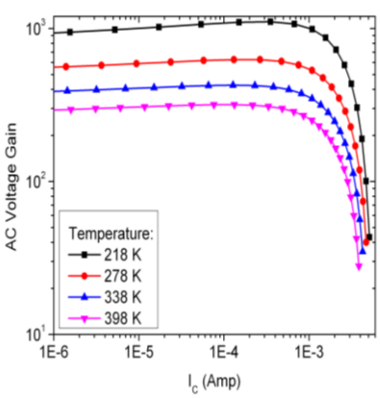

Fig. 5: AC voltage gain of SOI HBT

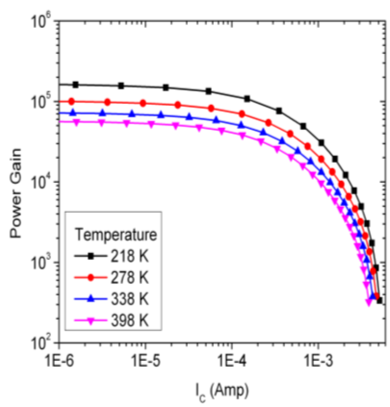

Fig. 6: Power gain of SOI HBT

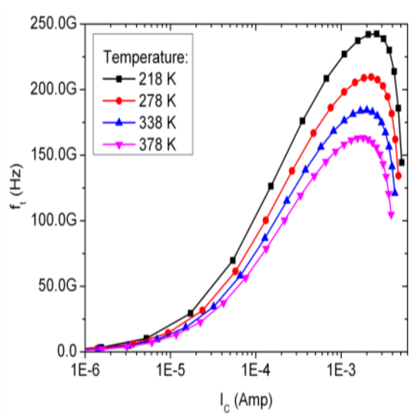

Fig. 7: Unity current gain frequency of HBT