

Comparative Study of Si₃N₄ and HfO₂/Si₃N₄ Stacked Trapping Layer on Junctionless Poly-Si Flash Memory Device

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Abstract: Effects of Si₃N₄ trapping layer (NTL) and HfO₂/Si₃N₄ bandgap-engineered trapping layer (BETL) on junctionless (JL) polycrystalline-based flash memory devices are investigated in this work. The programming speed is clearly improved by BETL but the erasing speed is only slightly improved. JL device with BETL performs better retention characteristics since the conduction band offset between Si₃N₄ and HfO₂ can reduce the leakage of trapped charges in HfO₂. The endurance characteristics of BETL sample is similar to that of NTL one, because both JL devices are less sensitive to interface state generation.

Introduction: For lower cost and higher device density, polycrystalline-Si (poly-Si) flash memory cell technology is regarded as a promising candidate for three-dimensional (3-D) NAND flash architecture. Since the doping control of source/drain (S/D) junction formation is difficult in 3-D architecture, an innovative junction formation process is necessary. A JL device is proposed by homogeneously doping S/D and channel, which is easily fabricated and free from S/D junctions [1]. Most studies about JL flash devices are based on NTL. The programming speeds of JL devices are improved by the electron-rich channel, but their erasing speeds are sacrificed due to the less hole generation. Effects of HfO₂/Si₃N₄ BETL on bulk planar devices and NW channel devices were reported to obtain better operating speeds and reliability performances [2]. However, these studies are only based on inversion mode flash devices. In this work, comparisons between NTL and HfO₂/Si₃N₄ BETL on JL flash devices with nanowire (NW) channels are studied.

Experimental: NTL and BETL devices are both fabricated on 6-inch Si (100) wafer. Firstly, four SiO₂ dummy fins with a height of 100 nm are formed by I-line lithography and reactive ion etching (RIE) process on Si₃N₄ buried layer. An 100-nm thick amorphous-Si is then deposited and transferred into poly-Si by solid-phase crystallization (SPC) process at 600 °C for 24 hours. Both samples are sent to perform Phosphorous implantation (at 30 keV to a dose of 1×10¹³ cm⁻²) and activation (900 °C for 30 s). S/D region is defined on two ends of dummy fins for all samples. Eight spacer NW channels are consistently formed with S/D region by precise RIE process control; SiO₂ dummy fins are removed by diluted HF to complete active region. 3.5 nm SiO₂ is grown as tunneling layer for both samples. 6 nm Si₃N₄ is deposited as NTL for one sample; 3 nm Si₃N₄ and 7 nm HfO₂ are sequentially deposited as BETL for another one. 18 nm Al₂O₃ is deposited as blocking layer, followed by TiN gate deposition. After gate region formation, both samples are sent to go through passivation and metallization processes, completed after sintering at 400 °C for 30 min.

Results and Discussion: Fig. 1 is the transmission electron microscopy (TEM) image of BETL device. The dielectric thicknesses are indicated and the width of a NW is ~25 nm. The transfer characteristics at V_{DS} = 0.5 V are shown in Fig. 2. The on-currents of both devices don't increase with gate bias, because the on-current of JL device is most related with the effective channel doping and less dependent on the increasing gate bias. Fig. 3 shows the programming speeds at V_{GS} = 14 V. The programming speed of JL device is improved by BETL due to the high trap density and lower conduction band level of HfO₂ as the band diagram indicates in Fig. 4 [2]. Fig 5 shows the erasing speed comparison of devices with a previous window of 2.5 V. The erasing speed is only slightly improved by BETL. It is because holes are less generated for JL device. Fewer holes are blocked by the barrier of HfO₂ during erasing operation such that the function of BETL is minor. Fig. 6 shows the retention characteristics tested at room temperature and 85 °C with a previous window of 2.5 V. The JL device with BETL performs better charge storage ability at both test conditions, which is because the conduction band offset between Si₃N₄ and HfO₂ can reduce the leakage of trapped charges in HfO₂. The endurance characteristics are shown in Fig. 7. Both devices perform good and similar cycling endurance because JL device is less sensitive to interface states due to the bulk conduction mechanism during cycling test.

Conclusions: Compared with NTL device, the programming speed of JL device is improved by BETL due to the lower conduction band level of HfO₂. The improvement of erasing speed by BETL is little since the function of BETL is not obvious when fewer holes are injected. Retention characteristics of JL device are improved by BETL due to the reduced charge leakage by the conduction band offset between HfO₂ and Si₃N₄. The endurance performance of JL device with BETL is similar with that with NTL. It is because JL device is less sensitive to interface states due to its bulk conduction mechanism.

References

[1] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.
 [2] C. Y. Chen, K. S. Chang-Liao, K. T. Wu and T. K. Wang, "Improved erasing speed in junctionless flash memory device by stacked trapping layer," *IEEE Electron Device Lett.*, vol. 34, pp. 993-995, Aug. 2013.

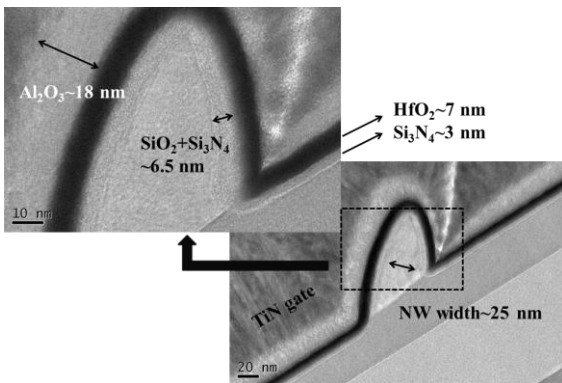


Fig. 1 Cross-section TEM image of JL device with BETL.

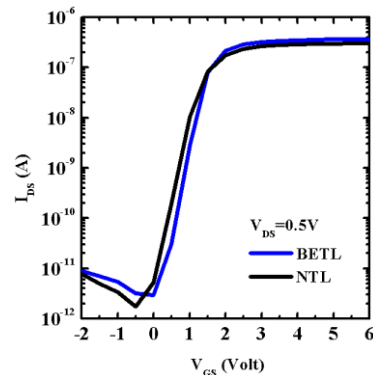


Fig. 2 Transfer characteristics of NTL and BETL devices.

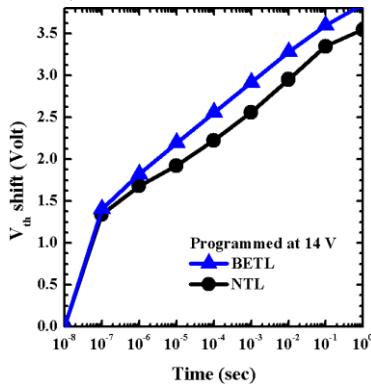


Fig. 3 Programming speed comparison of NTL and BETL devices.

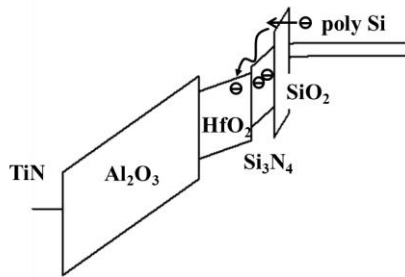


Fig. 4 Schematic energy band diagram of JL device with BETL at V_{GS} = 14 V

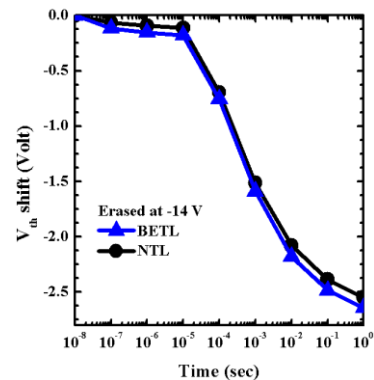


Fig. 5 Erasing speed comparison of NTL and BETL devices.

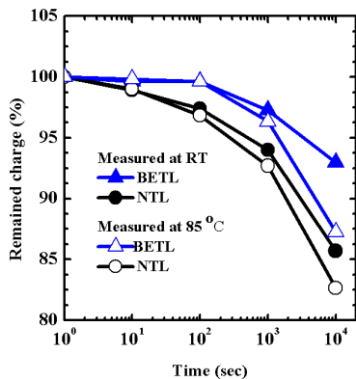


Fig. 6 Retention characteristics of NTL and BETL devices measured at different temperatures.

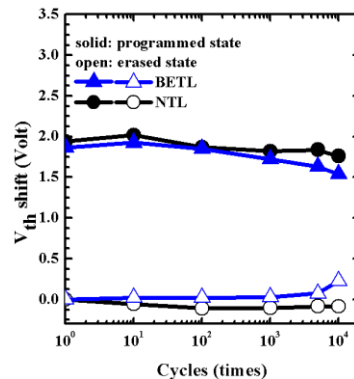


Fig. 7 Endurance characteristics of NTL and BETL devices with an initial window of 2 V.