Student Paper

IGZO TFTs on Aluminum Substrates

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The use of aluminum substrates for the fabrication of electronic devices, especially thin-film transistors (TFTs) offers significant merits for flat panel displays as well as for flexible electronics such as light weight, robustness, excellent barrier to moisture and compatibility with higher processing temperatures compared to polymer substrates. Similarly, oxide semiconductors such as a-IGZO are of special interest [1, 2, 3] since they offer better TFT performance and stability with respect to amorphous silicon or organic based TFTs.

We are reporting on characteristics of amorphous InGaZnO TFTs fabricated on aluminum substrates coated with an organic layer which serves to both planarize the aluminum surface and to provide an insulating coating for device fabrication upon it. We were able to overcome a challenge encountered by the thermal expansion coefficient mismatch between the coated aluminum substrate and PECVD gate dielectrics deposited at 270ºC which resulted in stress and adhesion problems. This problem was solved by RF-sputtering at room temperature a thin SiO_2 layer on top of the organic coating of the aluminum substrate before the onset of TFT fabrication.

The TFT device structure was a modified etch stop structure with S/D contact windows. First, a 140 nm layer of AlNd formed the gate electrodes. Then a stack of 110 nm SiO_2 was deposited by PECVD at 270℃ as the gate dielectric. 40 nm a-IGZO and 50 nm SiO_2 layers were then deposited by RF-magnetron to form channel and first passivation layers, respectively. Next, SiO_2 was dry etched by RIE system and IGZO layer was patterned by diluted HCL. After active etch, second passivation layer of SiO_2 with 50 nm thickness was deposited. It followed by gate pads and source/drain contact windows opening using dry etching technique. Finally, source and drain electrodes were formed by patterning a double layer of 70nm Mo and 100 nm AlNd by lift off process. The wafer was then annealed in N_2 ambient at 300℃ for a total of two hours.

Mobility was extracted from the maximum transconductance at V_{DS} = 0.1 V. TFTs with a 26 µm channel length and 40 µm channel width displayed an average field effect mobility of 8.6 $cm^2 V^{-1}s^{-1}$ (maximum of 13.3), threshold voltage of about 5 V, minimum off current less than 1 pA, and an on–off current ratio of more than 10^7 at V_{ds}=+10 V (maximum of more than 10^8). Prior to the final thermal annealing, the TFTs exhibited no modulation and a high current due to the high conductivity of the IGZO film; the thermal anneal in nitrogen ambient improved the device characteristics. Contrary to other reports we found that annealing in air ambient did not result in device improvement as the high IGZO conductivity was maintained.

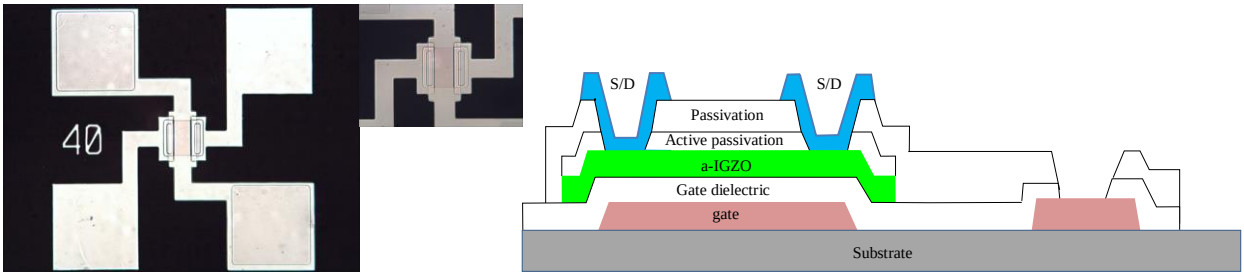

Figure 1 TFT layout with channel area of W40 µm and L26 µm (left), TFT Structure (Right)

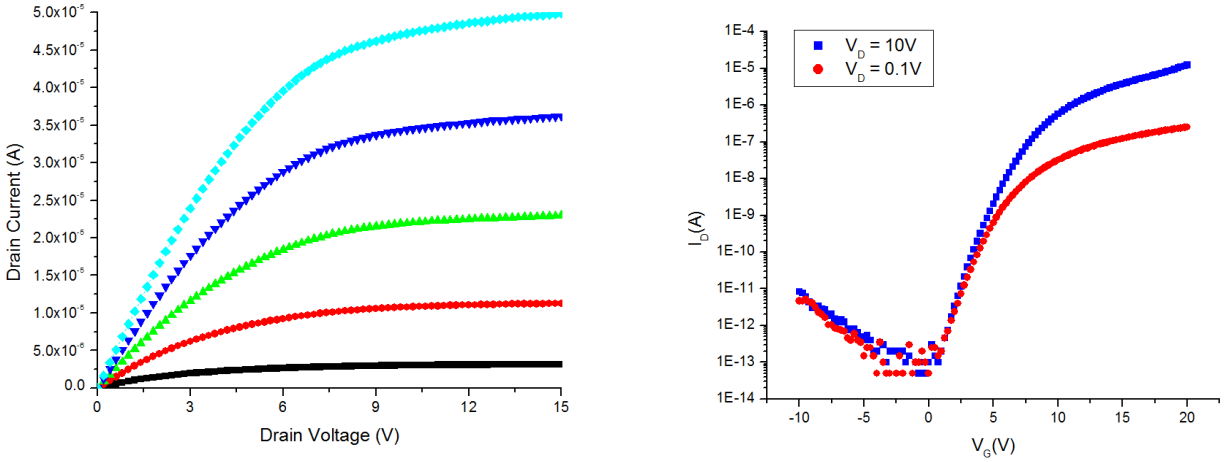

Figure 2 Output characteristics of TFT with length 14 µm and width 32 µm for Vg increment from 10 to 25 V (left), Transfer characteristics of TFT with length 5 µm and width 20 µm (Right)

References

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[3] Joon Seok Park, Wan-Joo Maeng, Hyun-Suk Kim, Jin-Seong Park, "Review of recent developments in amorphous oxide semiconductor thin-filmtransistor devices," Thin Solid Films, 520, 1679–1693,2012. (Journal Article)