InAs TFET optimized by means of TCAD to meet all the ITRS specs at V_{DD}= 0.5 V

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Abstract. A Dual-Metal-Gate (DMG) InAs Tunnel-FET (TFET) is devised and optimized through TCAD simulations to meet the ITRS specs of advanced multi-gate transistors at a reduced power supply of 0.5 V.

Introduction and preliminary TFET engineering. Band-To-Band-Tunneling (BTBT)-based TFET can provide inverse subthreshold slope (SS) of less than 60 mV/dec, thus enabling logic operation at V_{DD} lower than MOSFET's. In this work, we propose a novel DMG-TFET able to fulfill all the ITRS specs of multi-gate devices projected to year 2020. The InAs (low band-gap, low effective mass) vertical 10-nm radius gate-all-around nanowire (NW) reference device (RD) is depicted in Fig.1(a). A doping decay of 1 nm/dec is chosen to maximize the tunneling probability [1]. Also, we assume Al_2O_3 high-*k* dielectric as it is used in advanced InAs vertical FET technologies [2], and mid-gap metal gate. Optimization is performed by drift-diffusion-based TCAD employing a non-local BTBT model [3]. SRH and doping-dependent mobility are included in the simulations as well. A V_{DD} = 0.5 V, i.e. lower than prescribed by ITRS, is assumed. As a preliminary optimization, (i) a highly *p*-doped pocket is integrated in the channel to boost I_{ON} above 1 mA/µm; (ii) an intrinsic-drain layer (ID) is interposed between channel and drain to reduce ambipolarity, yielding the intrinsic-drain pocket device (ID-PD) of Fig.1(b). The turn-on curves of the RD and of an ID-PD optimized to fulfill ITRS LOP and HP specs, hereafter named OPT-ID-PD [4], are shown in Fig. 2, with currents normalized to the NW diameter. However, to target the LSTP specs as well, I_{OFF} must be further decreased by reducing the electric field at the upper pocket junction, where the off-state BTBT peak is located (see Fig. 3). Thus, the desired I_{OFF} is obtained by increasing the ID length to 100 nm (Fig. 4). However, to ensure both LSTP I_{OFF} and HP I_{ON} at V_{DD}= 0.5 V, SS must be further reduced. To this aim, we propose the novel DMG-TFET sketched in Fig.1(c). In DMG-TFET the gate is split in two, with the top gate (G2) wrapped around the upper pocket junction to better control BTBT in this region, aiming at reducing the electric field and at increasing the tunneling barrier at low V_{GS}.

Optimization of the Dual-Metal-Gate TFET. DMG-TFET is engineered by careful selection of the G2 length (LG2) and of the workfunction difference between G2 and InAs ($\Delta\Phi$). Simulation outcomes are: (i) LG2= 25 nm provides I_{OFF} below the LSTP limit as well as a lower SS (see Fig.5); (ii) $\Delta\Phi$= 100 meV significantly reduces SS (see Fig.6). Hereafter, the DMG device featuring LG2 = 25 nm and $\Delta\Phi$= 100 meV is referred to as optimal DMG (OPT-DMG). Figs.7 and 8 compare OPT-DMG and OPT-ID-PD off-states, showing BTBT reduction thanks to G2. Fig. 9 compares the turn-on of the optimized devices, highlighting the dramatic boosting of TFET characteristics. Also, OPT-DMG features higher output conductance (see Fig. 10), which is beneficial for rail-to-rail logic switching [5]. To provide further insights on OPT-DMG, Fig. 11 displays point SS, I_{ON}, and I_{ON}/I_{OFF} against I_{OFF}, comparing OPT-DMG with OPT-ID-PD. It is worth noticing that the point SS of OPT-DMG is lower than 60 mV/dec over more than five orders of magnitude of drain current, with a minimum value of 6 mV/dec sustained across one drain-current decade, or more. To conclude, OPT-DMG is benchmarked with respect to the ITRS in Tab.I. Remarkably, OPT-DMG fulfills all three 2020 ITRS specs.

Conclusions. We optimized an InAs DMG-TFET to fulfill all the ITRS specs for advanced multi-gate devices projected to year 2020. TCAD simulations show that the DMG architecture significantly lowers SS, thus yielding both LSTP compliant I_{OFF} and HP-compliant I_{ON} at V_{DD}= 0.5 V, corresponding to a 25% of reduction of static power consumption. Noticeably, DMG-TFET $I_{ON} \cong$ 2 mA/µm, which is the highest value reported in literature concerning TFETs simulated at ITRS-compliant, or lower V_{DD}.

References

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Acknowledgment

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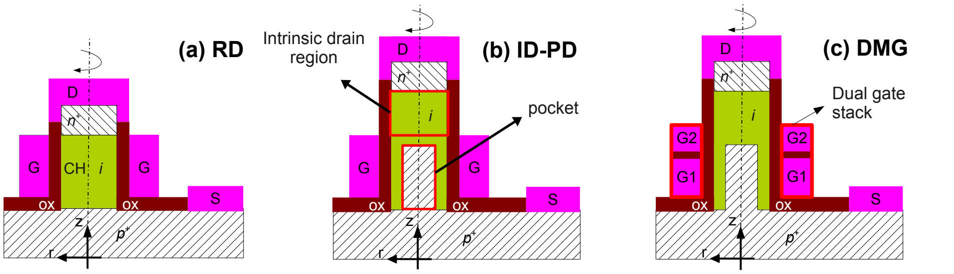

Fig. 1 Sketch (not drawn to scale) of device cross-sections (cylindrical symmetry is assumed). **(a)** Reference device (RD). The $p+$ substrate, doped at $5x10^{19}$ cm^{-3}, is the source; the intrinsic-channel (CH) length is 40 nm; the $n+$ drain is doped at $5x10^{18}$ cm^{-3}. **(b)** Intrinsic-drain pocket-device (ID-PD) with additional pocket and intrinsic drain region. Oxide thickness t_{ox} of RD is 1.8 nm (corresponding to LOP EOT), while the optimized device feature t_{ox}= 1.6 nm (HP EOT). **(c)** Dual-Metal-Gate (DMG). In DMG, a gate splitting is devised, with a 3-nm gap between the upper gate (G2) and the lower gate (G1), which length is reduced to 30 nm to accommodate G2.

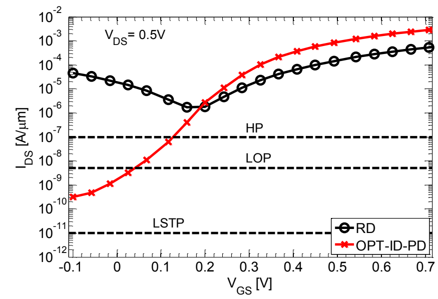

Fig.2 Turn-on characteristics of RD and OPT-ID-PD integrating a 35 nm-long and 6 nm-radius $p+$ pocket with doping of $7x10^{19}$ cm^{-3}, and a 70nm-long intrinsic drain. Dashed lines: I_{OFF} specs of HP, LOP, and LSTP.

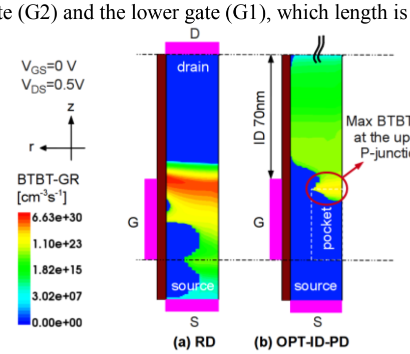

Fig. 3 Colormap of Band-to-Band-Tunneling generation rate (BTBT-GR) of **(a)** RD and **(b)** OPT-ID-PD in off-state (geometry not to scale, half of cross section shown).

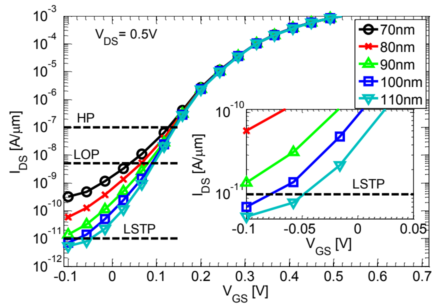

Fig. 4 Turn-on characteristics of ID-PD for various ID lengths. The minimum ID length fulfilling LOP and HP I_{OFF} specs, (the goal of OPT-ID-PD [4]), is 70 nm. A minimum ID length of 100 nm is instead needed to intercept the LSTP I_{OFF} spec (see inset).

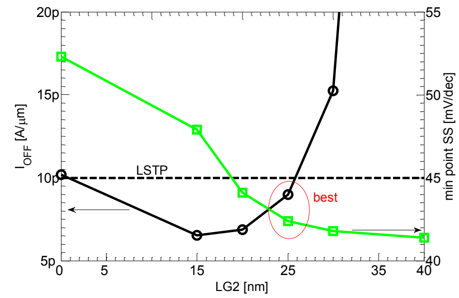

Fig. 5 Optimization of the upper-gate length of DMG, named LG2. I_{OFF} (left, circles) and minimum point SS (right, squares), as a function of LG2. The optimal LG2 is 25 nm, which features the lowest min point SS while, at the same time, fulfilling the LSTP I_{OFF} spec.

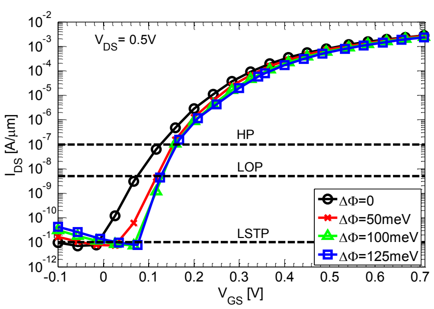

Fig. 6 Turn-on characteristics of DMG with varying $\Delta\Phi$. Increasing $\Delta\Phi$ yields a significant reduction of SS while I_{OFF} is constant. For $\Delta\Phi > 100$ mV, SS does not decrease further and ambipolarity increases owing to higher field.

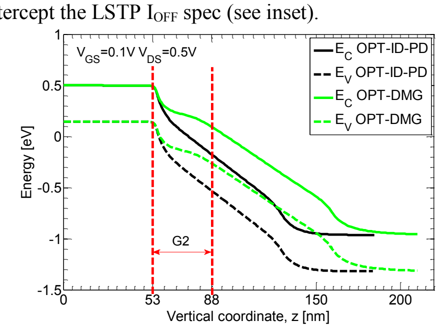

Fig. 7 Band diagrams in vertical direction (z) taken at the NW center (r= 0) for OPT-ID-PD (black) and OPT-DMG (green) in off-state. G2 extends between the vertical dashed lines (i.e. from z= 53 nm to z= 88 nm).

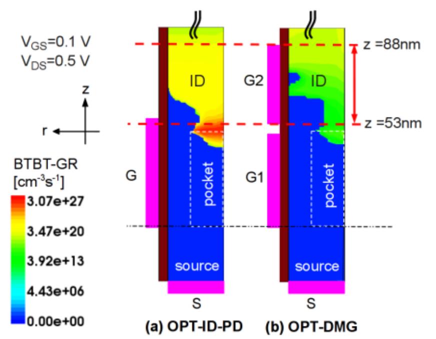

Fig. 8 Colormap of BTBT-GR for OPT-ID-PD **(a)**, and of OPT-DMG **(b)** in off-state (geometry not to scale).

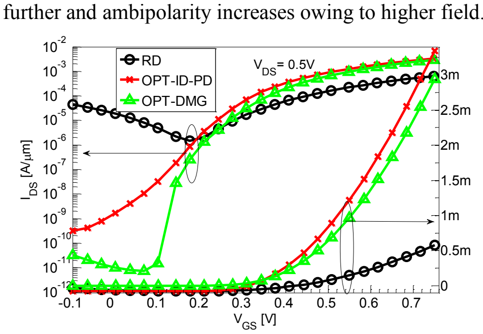

Fig. 9 Turn-on characteristics of RD, OPT-ID-PD and OPT-DMG (LG2 = 25 nm, $\Delta\Phi$ = 100 mV).

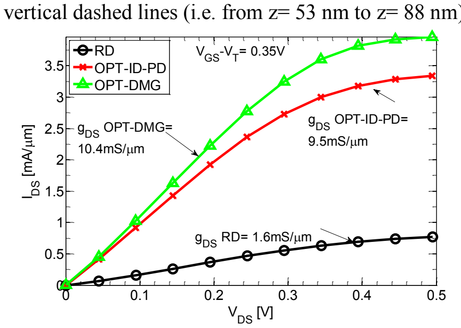

Fig. 10 Output characteristics of RD, OPT-ID-PD, and OPT-DMG simulated at V_{GS}= V_T + 0.35V (threshold voltage V_T corresponding to maximum of d^2I_{DS}/dV_{GS}^2).

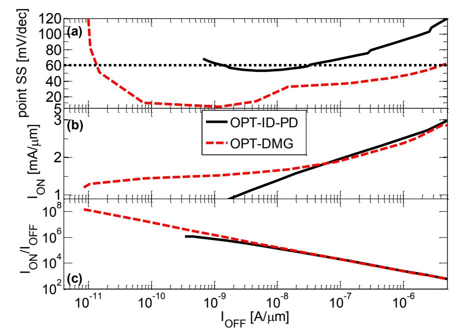

Fig. 11 **(a)** Point SS, **(b)** I_{ON}, and **(c)** I_{ON}/I_{OFF} vs. I_{OFF} for OPT-ID-PD (solid lines) and for OPT-DMG (dashed).

	ITRS (2020)			**OPT-DMG TFET**		
	LSTP	**LOP**	**HP**	**LSTP**	**LOP**	**HP**
V_{DD} [V]	0.67	0.53	0.68	0.5	0.5	0.5
I_{OFF} [nA/μm]	0.01	5	100	0.01	5	100
I_{ON} [mA/μm]	0.600	0.784	1.916	1.322	1.650	1.985

Tab.I Benchmarking of OPT-DMG TFET vs. ITRS specs referred to year 2020 for multi-gate transistors. To extract parameters, I_{OFF} is fixed to the ITRS prescribed value for each application, assuming that curve minimum can be shifted to V_{GS}=0 V by tuning the gate workfunction; then on-state performance is determined by applying V_{DD}=0.5V.